CLAIMS

We Claim:

1. An apparatus comprising:

a memory to couple to a data bus to transfer data between said memory and bus in response to a command signal received to initiate the data transfer and a flag signal received to complete the data transfer; and

a timing unit coupled to receive the command signal, flag signal and a memory select signal, said timing unit to generate a trigger signal in response to the flag signal to execute the data transfer, if the command signal indicates a command to transfer data and the memory select signal indicates that said memory is selected for the data transfer.

2. The apparatus of claim 1 wherein said timing unit includes a table entry to maintain record of the command signal, memory select signal and the flag signal, so that an indication of a presence of all three signals causes the trigger signal to be generated to execute the data transfer.

3. The apparatus of claim 2 wherein the table entry is to be cleared after receiving the flag signal to allow said table entry to receive next set of command, memory select and flag signals to determine if the trigger signal is to be generated for said memory with the next set of command, memory select and flag signals.

4. The apparatus of claim 3 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

5. The apparatus of claim 3 wherein said memory is a dynamic-random-access-memory, DRAM.

6. The apparatus of claim 1 wherein said timing unit includes table entries arranged in a queue to maintain record of occurrences of the command signal, memory select signal and the flag signal, so that an indication of a presence of all three signals for a given set of command, memory select and flag signals are recorded in a given set of entries and causes the trigger signal to be generated to execute the data transfer.

7. The apparatus of claim 6 further includes a first pointer to point to a next set of entries after recording the occurrence of the command and memory select signals; and a second pointer to point to the next set of entries after recording the occurrence of the flag signal.

8. The apparatus of claim 7 wherein the entries of a corresponding set of entries are to be cleared after receiving the flag signal to allow said set of entries to cycle through as queue entries.

9. The apparatus of claim 8 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

10. The apparatus of claim 8 wherein said memory is a dynamic-random-access-memory, DRAM.

11. An apparatus comprising:

a memory to couple to a data bus to transfer data between said memory and bus in response to a command signal received to initiate the data transfer and a flag signal received to complete the data transfer, said memory to operate as one of a plurality of

memories, wherein a flag signal operating in timing order with the command signal indicates timing when the data transfer is to occur following the command signal; and

a timing unit coupled to receive the command signal, flag signal and a chip select signal, said timing unit to generate a trigger signal in response to the flag signal to execute the data transfer, if the command signal indicates the data transfer and the chip select signal indicates that said memory is selected for the data transfer.

12. The apparatus of claim 11 wherein the command signal is a read command or write command.

13. The apparatus of claim 12 wherein said timing unit includes table entries to maintain record of the command signal, chip select signal and the flag signal, so that a command entry is to be set when the read or write command is present, a chip select entry is to be set when the chip select signal is present and the flag entry is to be set when the flag signal is present, the trigger signal to be generated to execute the data transfer when all three respective entries are set.

14. The apparatus of claim 13 wherein the respective table entries are to be cleared after receiving the flag signal to allow the entries to receive a next set of command, chip select and flag signals.

15. The apparatus of claim 14 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

16. The apparatus of claim 14 wherein said memory is a dynamic-random-access-memory, DRAM.

17. The apparatus of claim 13 wherein said timing unit includes table entries arranged in a queue to maintain record of occurrences of the command, chip select and the flag signals, so that subsequent occurrences of all three signals is to be recorded.

18. The apparatus of claim 17 further includes a first pointer to point to a next set of entries after recording the occurrence of the command and chip select signals; and a second pointer to point to the next row of entries after recording the occurrence of the flag signal.

19. The apparatus of claim 18 wherein said memory is a dynamic-random-access-memory, DRAM.

20. A system comprising:

a controller to generate a command signal to initiate data transfer and also to generate a flag signal to time completion of the data transfer;

a memory coupled to said controller to receive the command signal and complete the data transfer in response to the flag signal;

a bus coupled to said memory to transfer data between said memory and bus in response to the flag signal;

said controller to generate the command signal during a first clock period, along with a corresponding chip select signal to activate said memory to perform the data transfer, and the flag signal following the data transfer command signal at a later clock period; and

said memory including a timing unit coupled to receive the command signal, flag signal and a chip select signal, said timing unit to generate a trigger signal in response to

the flag signal to execute the data transfer, if the command signal indicates the data transfer and the chip select signal indicates that said memory is selected for the data transfer.

21. The system of claim 20 wherein said timing unit includes table entries to maintain record of the command signal, chip select signal and the flag signal, so that a command entry is to be set when the read or write command is present, a chip select entry is to be set when the chip select signal is present and the flag entry is to be set when the flag signal is present, the trigger signal to be generated to execute the data transfer when all three respective entries are set.

22. The system of claim 21 wherein the respective table entries are to be cleared after receiving the flag signal to allow the entries to receive a next set of command, chip select and flag signals.

23. The system of claim 22 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

24. The system of claim 22 wherein said memory is a dynamic-random-access-memory, DRAM.

25. A method comprising:

issuing a command signal to perform a read or write operation;

issuing a chip select signal to select a particular memory device to perform a data transfer for the read or write operation;

generating a flag signal subsequently in response to the issuing of the command signal to completes the data transfer; and

capturing occurrences of the command signal, chip select signal and the flag signal in a memory device and generating a trigger signal when command, chip select and flag signals present are captured for the memory device, the trigger signal to execute the data transfer to complete the read or write operation in the memory device.

26. The method of claim 25 wherein the command signal is driven in a same clock period the chip select signal is asserted.

27. The method of claim 26 wherein said capturing the signals are achieved by setting entries on occurrence of the signals.

28. The method of claim 27 further including the clearing of the entries after occurrence of the flag signal.

29. The method of claim 26 wherein said capturing of the signals is performed in a dynamic-random-access-memory, DRAM.